In the Claims:

1. (Original) A memory device comprising:

a capacitor comprising a lower electrode, an upper electrode and a dielectric layer interposed between the lower electrode and the upper electrode; and

a multi-layered encapsulating layer surrounding the capacitor, the multi-layered encapsulating layer comprising a first blocking layer which is annealed and a first protection layer formed on the annealed first blocking layer, the first blocking layer and the first protection layer being formed of the same material.

2. (Original) The memory device of claim 1, wherein the first blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the first protection layer.

3. (Original) The memory device of claim 1, wherein the first blocking layer is a metallic oxide layer.

4. (Original) The memory device of claim 2, wherein the first blocking layer is a metallic oxide layer.

5. (Currently Amended) The memory device of claim 3, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

6. (Original) The memory device of claim 1, wherein the thickness of the first blocking layer is 10-50% of the thickness of the first protection layer.

7. (Original) The memory device of claim 6, wherein the first blocking layer is formed of Al_2O_3.

8. (Original) The memory device of claim 7, wherein the thickness of the first blocking layer is 10-15 Å, and the thickness of the first protection layer is about 100 Å.

9. (Original) The memory device of claim 1, wherein the first blocking layer and the first protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method or a plasma chemical vapor deposition method.

10. (Original) The memory device of claim 1, further comprising an interlayer insulation layer formed on the first protection layer and a second encapsulating layer formed on the interlayer insulation layer, the second encapsulating layer comprising a second blocking layer which is annealed and a second protection layer formed on the second blocking layer, the second blocking layer and the second protection layer comprising the same material.

11. (Original) The memory device of claim 10, wherein the second blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the second protection layer.

12. (Original) The memory device of claim 10, wherein the second blocking layer is a metallic oxide layer.

13. (Original) The memory device of claim 11, wherein the second blocking layer is a metallic oxide layer.

14. (Currently Amended) The memory device of claim 12, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

15. (Original) A memory device comprising:

a lower electrode;

a dielectric layer formed on a predetermined portion of the surface of the lower electrode;

a spacer layer formed on the lower electrode, the spacer layer comprising a blocking spacer directly contacting a sidewall of the dielectric layer and a protection spacer formed on the blocking spacer;

an interlayer insulation layer formed on the lower electrode to contact the protection spacer;

an upper electrode formed on the dielectric layer; and

a multi-layered encapsulating layer surrounding the interlayer insulation layer, the spacer layer and the upper electrode, the multi-layered encapsulating layer comprising a first blocking layer which is annealed and a first protection layer formed on the annealed first blocking layer, the first blocking layer and the first protection layer being formed of the same material.

16. (Original) The memory device of claim 15, wherein the first blocking layer has an enough thickness to block diffusion of hydrogen generated during the formation of the first protection layer.

17. (Original) The memory device of claim 15, wherein the first blocking layer is a metallic oxide layer.

18. (Original) The memory device of claim 16, wherein the first blocking layer is a metallic oxide layer.

19. (Currently Amended) The memory device of claim 17, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

20. (Original) The memory device of claim 16, wherein the first blocking layer is formed of Al_2O_3.

21. (Original) The memory device of claim 20, wherein the thickness of the first blocking layer is 10-15 Å, and the thickness of the first protection layer is about 100 Å.

22. (Original) The memory device of claim 15, wherein the first blocking layer and the first protection layer are formed by an atomic layer deposition method, a low pressure chemical vapor deposition method, a high pressure chemical vapor deposition method or a plasma chemical vapor deposition method.

23. (Original) The memory device of claim 15, further comprising a second interlayer insulation layer formed on the first protection layer and a second encapsulating layer formed on the second interlayer insulation layer, the second encapsulating layer comprising a second blocking layer which is annealed and a second protection layer formed on the second blocking layer, the second blocking layer and the second protection layer comprising the same material.

24. (Original) The memory device of claim 23, wherein the second blocking layer has sufficient thickness to block diffusion of hydrogen generated during the formation of the second protection layer.

25. (Original) The memory device of claim 23, wherein the second blocking layer is a metallic oxide layer.

26. (Original) The memory device of claim 24, wherein the second blocking layer is a metallic oxide layer.

27. (Currently Amended) The memory device of claim 25, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

28. (Original) The memory device of claim 15, wherein the blocking spacer has an enough thickness to block diffusion of hydrogen generated during the formation of the protection spacer.

29. (Original) The memory device of claim 15, wherein the blocking spacer is a metallic oxide layer.

30. (Original) The memory device of claim 28, wherein the blocking spacer is a metallic oxide layer.

31. (Currently Amended) The memory device of claim 30, wherein the metallic oxide layer is formed of one selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

32. (Currently Amended) An integrated circuit, comprising:

a ferroelectric dielectric region on a substrate;

a first metal oxide layer directly on a surface of the ferroelectric dielectric region; and

a nonconductive second metal oxide layer on the first metal oxide layer,

wherein the first metal oxide layer is configured to enable a remnant polarization of the ferroelectric dielectric region to increase during an annealing of the substrate before formation of the second metal oxide layer.

33. (Original) An integrated circuit according to Claim 32, wherein the first metal oxide layer is thick enough to substantially impede diffusion of hydrogen into the ferroelectric dielectric region.

34. (Currently Amended) An integrated circuit according to Claim 32:

wherein the first metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2; and

wherein the second metal oxide layer comprises a metal oxide selected from the group consisting of Al_2O_3, TiO_2, ZrO_2, [[Ta_5O_3]] $\underline{T_2O_5}$ and CeO_2.

35. (Original) An integrated circuit according to Claim 32, wherein the second metal oxide layer is thicker than the first metal oxide layer.

36. (Original) An integrated circuit according to Claim 35, wherein the second metal oxide layer is at least about twice as thick as the first metal oxide layer.

37. (Original) An integrated circuit according to Claim 36, wherein the second metal oxide layer is less than about ten times as thick as the first metal oxide layer.

38. (Original) An integrated circuit according to Claim 35, wherein the first and second metal oxide layers each are Al_2O_3 layers.

39. (Original) An integrated circuit according to Claim 38, wherein the first metal oxide layer has a thickness in range from about 10 Å to about 15 Å and wherein the second metal oxide layer has a thickness greater than about 50 Å.

40. (Original) An integrated circuit according to Claim 32, wherein the ferroelectric dielectric region is a dielectric of a capacitor.

41. (Original) An integrated circuit according to Claim 32, wherein the ferroelectric dielectric region comprises a ferroelectric material selected from the group consisting of $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr, Ti)O_3, $SrBi_2Ta_2O_9$, (Pb, La)(Zr, Ti)O_3 and $Bi_4Ti_3O_{12}$.

42.-72. (Canceled)